



TRANSMITTAL FORM

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Application Number	10/786,010
Filing Date	02/26/2004
First Named Inventor	Pierte ROO
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	MP0039.C1

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Total number of pages in this submission including transmittal 4^{\star}		Attorney Docket Number		MP0039.C1		
ENCLOSURES (check all that apply)						
Fee Transmittal Form Fee Attached - Check Amendment / Reply After Final Affidavits/declaration(s) Extension of Time Request Express Abandonment Request Information Disclosure Statement with PTO 1449s and cited references Certified Copy of Priority Document(s)	Assignm (for an A) Drawing Licensin Petition Petition Provisio Change Address Termina Requesi CD, Nut	ment Papers Application) g(s) ng-related Papers to Convert to a conal Application of Attorney, Revocat e of Correspondence	ition e	After Allowance Communication to TC Appeal Communication to Board of Appeals and Interferences Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) Proprietary Information Status Letter Other Enclosure(s) (identify below):		
Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53	REMARKS					
SIGNATUF	RE OF APPLI	ICANT, ATTORNE	EY. OR AC	GENT		
Firm Name KATTEN MUCHIN ROSENMAN, L						
Signature	Andrew	1. Bate	wan	-		
Printed Name Andrew J. Bateman		0				
Reg. No. 45,573			Date:	08/11/2005		
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In re Application of: AUG 1 1 2005 Pierte ROO Application No.: 10/786,016 PADEN Filed: February 26, 2004

ACTIVE RESISTIVE SUMMER FOR A TRANSFORMER HYBRID

Examiner: Unknown

Group Art Unit: Unknown

Date: August 11, 2005

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

For:

In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449s and to the attached copies of any non-U.S. Patent or literature references cited thereon.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, if deemed necessary, the Commissioner is authorized to charge the IDS fee of \$180.00 to Deposit Account No. 50-1710.

Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

IP Docket Katten Muchin Rosenman, LLP 1025 Thomas Jefferson St., NW East Lobby, Suite 700 Washington, DC 20007-5201 Facsimile No.: (202) 298-7570

Respectfully submitted, KATTEN MUCHIN ROSENMAN, LLP

Andrew J. Baterhan Registration No. 45,573

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U.S. PATENT AND TRADEMARK OFFICE			MP0039.C1		10/786,010		
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U.S. PATENT	DOCUMENTS	AUG 11 2005 =					
*EXAMINER INITIALS	EXAMINER DOCUMENT NUMBER PADEMANTE		NAME CLASS		SUBCLASS	FILING DATE	
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ATTORNEY DOCKET NO. **APPLICATION NO.** FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE MP0039.C1 10/786,010 **APPLICANT** LIST OF REFERENCES CITED BY APPLICANT Pierte ROO **FILING DATE GROUP** DATE SUBMITTED TO USPTO: August 11, 2005 02/26/2004 Unknown OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.) **INITIALS** Rao, Short Course: Local Area Networks Razavi, Principles of Data Conversion System Design Mano, Digital Logic and Computer Design Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS Johnson, et al., THAM 11.2: A Variable Delay Line Phase Locked Loop for CPU-Coprocessor Synchronization Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode Garlepp, et al., A Portable Digital DLL Architecture for CMOS Interface Circuits Lin, et al., A Register-Controller Symmetrical DLL for Double-Data-Rate DRAM Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm2

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DATE CONSIDERED

EXAMINER